CS 489 / 698: Software and Systems Security

Module 9: Hardware Security side-channel attacks and countermeasures

Meng Xu (University of Waterloo) Winter 2024





2 Timing-based cache side channels

3 Covert channels

- Install a malware (spyware) on the victim's computing device
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- Side channels
 - e.g., timing, bandwidth, power, etc.

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Wherever he steps, whatever he touches, whatever he leaves, even unconsciously, will serve as a silent witness against him. Not only his fingerprints or his footprints, but his hair, the fibres from his clothes, the glass he breaks, the tool mark he leaves, the paint he scratches, the blood or semen he deposits or collects. All of these and more, bear mute witness against him. This is evidence that does not forget.

— Paul L. Kirk

Locard's exchange principle (in code execution)

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Wherever he steps Every CPU instruction executed, whatever he touches every memory access, whatever he leaves every IO operation, even unconsciously, will serve as a silent witness against him the code.

My personal story



Examples of side channels

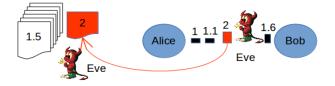
- Bandwidth consumption
- Reflections
- Cache-timing channels

Bandwidth consumption: scenario



- Eve observes communication going via Alice's Router
- Alice accesses health forum via encrypted connection
- Eve knows that Alice connects to health forum
- But cannot decrypt downloaded content

Bandwidth consumption: attack



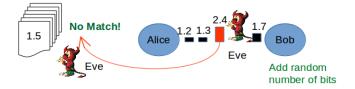
- Eve determines size of all pages on health forum
- Eve measures size of Alice's downloaded pages
- Likely: Eve can uniquely map download to page
- This attack is called webpage fingerprinting
 - or website fingerprinting, when targeting landing pages

Bandwidth consumption: defense

• Pad all pages to common size (inflexible + inefficient 🐸)

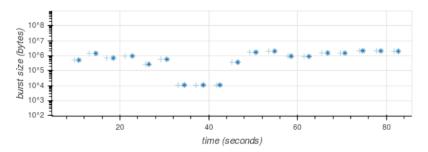


- Dynamic personalized websites
- (Finally a benefit of targeted advertisement)



Bandwidth consumption: another example

- Re-identification of Netflix video streaming
- Burst sizes of a streamed scene of "Reservoir Dogs"
 - Very similar, even when watched over different networks



Schuster et al., USENIX SEC '17

Reflections: scenario

- Alice types her password on a device in a public place
- Alice hides her screen
- But there is a reflecting surface close by







Reflections: attack

- Eve uses a camera and a telescope
- Off-the-shelf: less than CA\$2,000
- Photograph reflection of screen through telescope
- Reconstruct original image
- Distance: 10-30 m
- Depends on equipment and type of reflecting surface

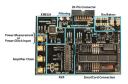
Reflections: defense



Other potential attack vectors

- Timing computations
- Electromagnetic emission
- Sound emissions
- Power consumption
- Differential power analysis
- Differential fault analysis







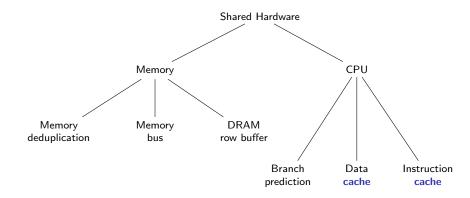
Outline



2 Timing-based cache side channels

3 Covert channels

Common hardware shared



Cache timing side channels

- Modern architectures use caches to speed up memory access
 - Main memory access is slow. Cache access is faster.
 - Caches are micro-architectural objects, not architectural: programs typically unaware of caches.
 - Caches are shared: by timing cache access, a process can learn information about data used by another.

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- Caches are shared: by timing cache access, a process can learn information about data used by another.

- Micro-architectural features like speculative and out-of-order execution can be exploited to leak information via caches.
 - Spectre and Meltdown attacks (2017)

Why targeting cache?

- Shared across cores
 - agonistic to kernel, hypervisor, and emulators!
- Observable effect
 - data/instruction is cached \rightarrow cache hit \rightarrow fast
 - data/instruction is not cached \rightarrow cache miss \rightarrow slow

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\implies cross-core attacks!

Measuring time differences caused by cache

- build two cases: cache hits and cache misses
- Itime each case many times (get rid of noise)
- Int a histogram
- Ind a threshold to distinguish the two cases

 Covert 0000

Side note: how to measure timing accurately?

rdtsc instruction: cycle-accurate timestamps

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```
t1 := rdtsc
\langle \dots \text{operation} \dots \rangle
t2 := rdtsc
duration := t2 - t1
```

rdtsc instruction: cycle-accurate timestamps

```
t1 := rdtsc
{ ... operation ... }
t2 := rdtsc
duration := t2 - t1
```

Q: Is this correct? Do you measure what you think you measure?

A: Out-of-order execution

```
t1 := rdtsc
\langle \dots \text{operation} \dots \rangle
t2 := rdtsc
duration := t2 - t1
\langle \dots \text{other-ops} \dots \rangle
```

A: Out-of-order execution

t1 := rdtsc	t1 := rdtsc
$\langle \dots operation \dots \rangle$	$\langle \ \dots \text{other-ops} \ \dots \rangle$
t2 := rdtsc	t2 := rdtsc
duration := t2 - t1	duration := $t2 - t1$
$\langle \ \dots \text{other-ops} \ \dots \rangle$	$\langle \dots operation \dots \rangle$

A: Out-of-order execution

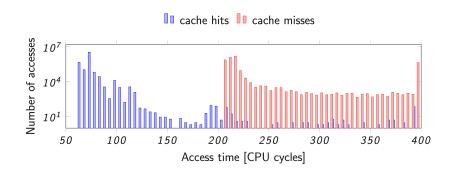
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duration := $t2 - t1$	duration := t2 - t1	$\langle \dots \text{ other-ops } \dots \rangle$
$\langle \ \dots $ other-ops $\dots \rangle$	$\langle \dots operation \dots \rangle$	duration := t2 - t1

Side note: how to measure timing accurately?

- use pseudo-serializing instruction rdtscp (recent CPUs)
- and/or use serializing instructions like cpuid
- and/or use fences like mfence

How to Benchmark Code Execution Times on Intel IA-32 and IA-64 Instruction Set Architectures White Paper, December 2010.

Timing difference on cache hit/miss



Cycle difference on cache hit/miss

On current Intel CPUs:

- L1 cache: 4 cycles
- L2 cache: 12 cycles
- L3 cache: 26-31 cycles
- DRAM memory: > 120 cycles

(Unprivileged) cache maintenance

User programs can (voluntarily) optimize cache usage:

- prefetch: suggest CPU to load data into cache
- clflush: throw out data from all caches
- ... based on virtual addresses

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This is the enabler of any cache-based attack:

Attacker monitors its own activity to find cache accessed by victim.

A concrete scenario

- You run a secret program on machine, and the program does one of two things
 - encrypt()
 - decrypt()
- You do not want anyone to know whether your program is encrypting a message or decrypting a message.
 - assuming trust in operating system and hardware
- The binary of your program is available.

A concrete scenario

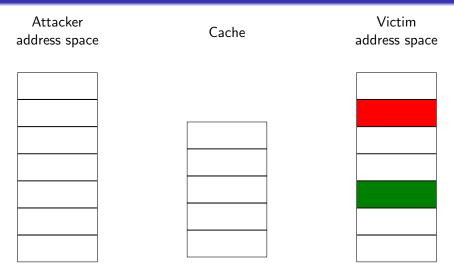
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- Attackers can run their programs on the same machine.
- Their goal is to infer which operation your program is running.

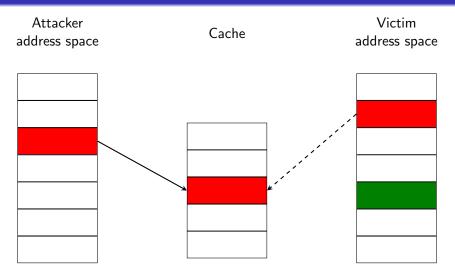
Access-driven attacks

• Flush+Reload

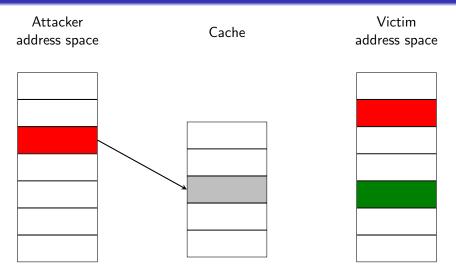
• Prime+Probe



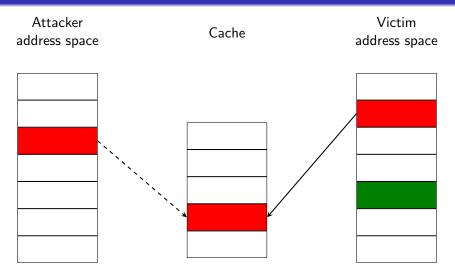
Init: victim program loaded while cache is empty



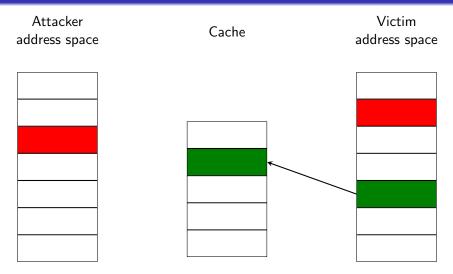
Step 1: attacker loads the encrypt() code into its address space



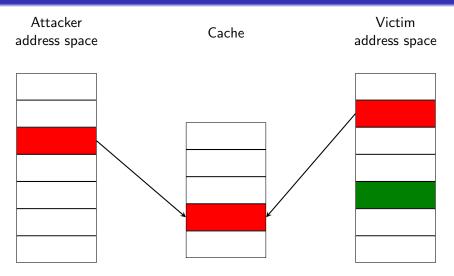
Step 2: attacker flushes the shared cache



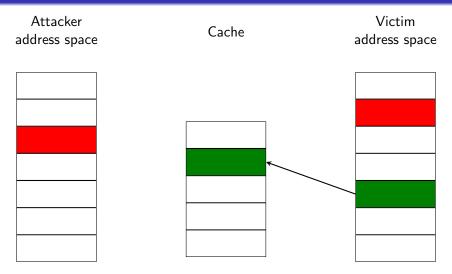
Step 3(a): victim performs operation encrypt()



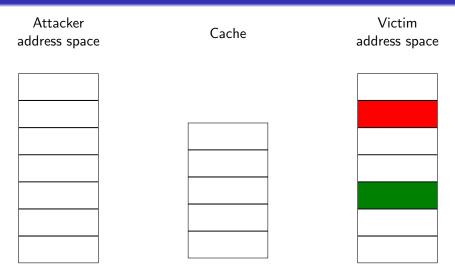
Step 3(b): victim performs operation decrypt()



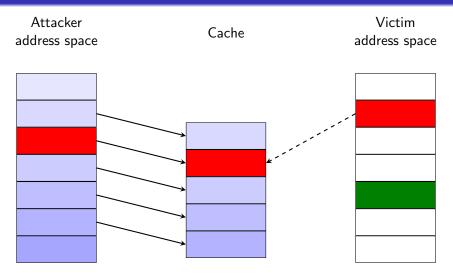
Step 4: attacker calls encrypt() after step $3(a) \implies fast!$



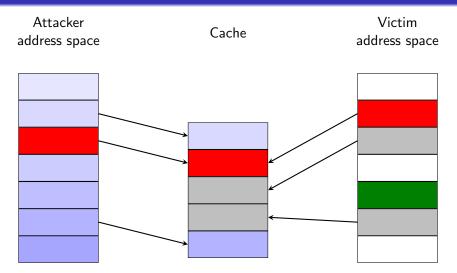
Step 4: attacker calls encrypt() after step $3(b) \implies slow!$



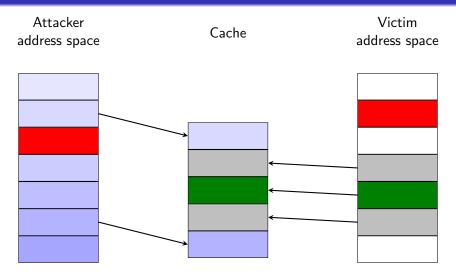
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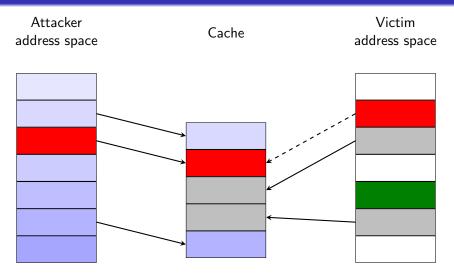
Step 1: attacker fills *all* available cache (prime)



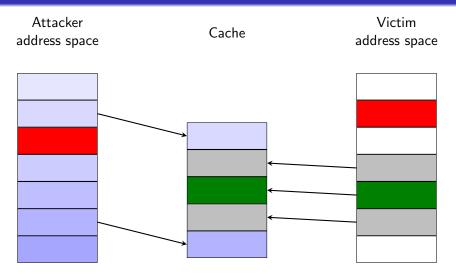
Step 2(a): victim evicts cache lines while performing operation encrypt()



Step 2(b): victim evicts cache lines while performing operation decrypt()



Step 3: attacker calls encrypt() after step $2(a) \implies fast!$



Step 3: attacker calls encrypt() after step $2(b) \implies slow!$

• Fuse the functionalities into a single code piece

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1 if (flag) { encrypt_instruction_1(); }
2 else { decrypt_instruction_1(); }
3 if (flag) { encrypt_instruction_2(); }
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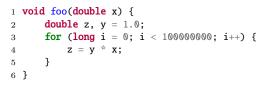
• Voluntary cache eviction

Both at the expense of performance overhead.

More systematic countermeasures

- Use constant-time programming techniques
- Eliminate secret-dependent execution or branches
- Hide/blind inputs

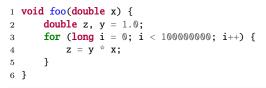
More on constant time techniques



Q: Which of the following execution is faster?

- foo(1.0)
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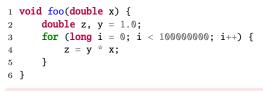
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Some observations:

- Avoid variable-time instructions
- If-statements on secrets are unsafe
- There are tools to help but most constant-time code is still

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What information can/cannot be transmitted through a channel may be determined by a policy/guidelines/physical limitations, etc.

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- Eve can "hide" the sensitive data in that report!
 - e.g., modifications to spacing, wording, or the statistics itself

\langle End \rangle